- BiCMOS Design Significantly Reduces I_{CCZ}
- 3-State True Outputs Drive Bus Lines Directly
- High-Impedance State During Power Up and Power Down
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (N)

DIR 19 OE A1 2 18 B1 А2 П 3 А3 [4 17 B2 **B**3 5 A4 📙 16 А5 П 15 ∏ B4 6 A6 [∏ B5 A7 🛮 8 13 B6 A8 🛮 9 12 B7 **∏** B8 GND [10

DW OR N PACKAGE (TOP VIEW)

description

This octal bus transceiver is designed for asynchronous communication between data

buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

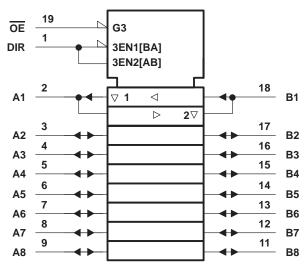
The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT245 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE

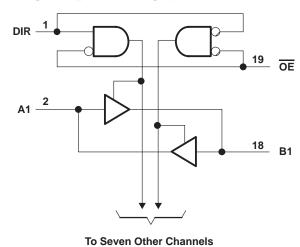
INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	X	Isolation

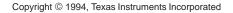
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	– 0.5 V to 7 V
Input voltage range, V _I (see Note 1)	– 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V _O	0.5 V to 5.5 V
Voltage range applied to any output in the high state, V _O	$\dots - 0.5 \text{ V to V}_{CC}$
Current into any output in the low state	128 mA
Operating free-air temperature range	– 40°C to 85°C
Storage temperature range	. – 65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	V
VIH	High-level input voltage		2			V
V _{IL}	Low-level input voltage			0.8	V	
lik	Input clamp current				-18	mA
	High level output ourrant	A1-A8			-3	mA
ІОН	High-level output current	B1-B8			-15	IIIA
la.	Low-level output current	A1-A8			24	mA
IOL	Low-level output current	B1-B8			64	ША
T _A	Operating free-air temperature		-40		85	°C

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS					
VIK		V _{CC} = 4.5 V,	I _I = -18 mA				-1.2	V
	Any A		I _{OH} = -1 mA		2.5	3.4		
Vон	Any A or B	V _{CC} = 4.5 V	IOH = -3 mA		2.4	3.3		V
	Any B		I _{OH} = -15 mA		2	3.1		
V	Any A	V 45V	I _{OL} = 24 mA			0.35	0.5	V
VOL	Any B	V _{CC} = 4.5 V	I _{OL} = 64 mA			0.42	0.55	V
	Power up	Va a 0 to 2 2 V	V _O = 2.7 V	<u></u>			70	μΑ
	Power up	$V_{CC} = 0$ to 2.3 V	V _O = 0.5 V	OE at 0.8 V			-0.65	mA
loz	Dawen dawe	V 4.0.V+c.0	V _O = 2.7 V	<u></u>			70	μΑ
	Power down	$V_{CC} = 1.8 \text{ V to } 0$	V _O = 0.5 V	OE at 0.8 V			-0.65	mA
. +	A and B	V 55V	V. EEV			1	mA	
11‡	DIR and OE	V _{CC} = 5.5 V,	V _I = 5.5 V			0.1	mA	
. +	A and B	Vac 55V	V: 0.7.V				70	
¹ _{IH} ‡	DIR and OE	V _{CC} = 5.5 V,	V _I = 2.7 V			20	μΑ	
	A and B	V 55V	V: 0.5.V			-0.65	A	
ΊL	DIR and OE	V _{CC} = 5.5 V,	V _I = 0.5 V			-1.2	mA	
	Any A	V 55V	V- 0	-60		-150	A	
los§	Any B	V _{CC} = 5.5 V,	VO = 0	-100		-225	mA	
ICCH	A-to-B	V _{CC} = 5.5 V				36	57	
ICCL	A-to-B	V _{CC} = 5.5 V				57	90	mA
I _{CCZ}		V _{CC} = 5.5 V				10	15	
Ci	OE and DIR	V _{CC} = 5 V,	V _I = 2.5 V or 0.5 V			7		pF
C.	A to B	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	Vi = 2.5 V or 0.5 V			9		n.E
C _{io}	B to A	V _{CC} = 5 V,	$V_{I} = 2.5 \text{ V or } 0.5 \text{ V}$			12		pF

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = C _L = 5 R1 = 5 R2 = 5 T _A = 2	50 pF, 500 Ω, 500 Ω,	C _L R1	= 50 pF, = 500 Ω, = 500 Ω	,	0°C	UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	1
^t PLH	A or B	B or A	1	6	1	7.2	1	7	ns
t _{PHL}	AUID	BULA	1.5	6.6	1.5	7.6	1.5	7	115
^t PZH	ŌĒ	A or B	1.5	9.4	1.5	11.2	1.5	10.9	ns
t _{PZL}	OE	AOIB	1.5	10.2	1.5	11.8	1.5	11.6	115
^t PHZ	ŌĒ	A or B	1.5	8.3	1.5	9.7	1.5	9.3	ns
^t PLZ		AUD	1.5	7.8	1.5	9.6	1.5	9.1	115

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



[†] All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current. § Not more than one output should be tested at a time, and the duration of the test should not exceed one second.





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp (3)
SN64BCT245DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN64BCT245NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN64BCT245NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN64BCT245NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

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to Customer on an annual basis.	



TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN64BCT245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN64BCT245NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN64BCT245DWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN64BCT245NSR	SO	NS	20	2000	346.0	346.0	41.0

MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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